

CLAIMS

What is claimed is:

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1 1. An apparatus, comprising:  
 2 a controller;  
 3 a hybrid switching element suitable for interpreting network data received from a  
 4 networking device and storage data received from a storage device;  
 5 a protocol accelerator suitable for utilizing a data storage addressing scheme; and  
 6 an error control component suitable for compensating for loss of at least one of a  
 7 network element and a data storage element;  
 8 wherein the error control component is communicatively coupled to the hybrid  
 9 switching element, protocol accelerator and controller so as to enable error  
 10 control coding including network and data storage.

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1 2. The apparatus as described in claim 1, wherein data is addressed utilizing a 128  
 2 bit addressing scheme.

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1 3. The apparatus as described in claim 2, wherein the addressing scheme is at least  
 2 one of IPv6 and IPv4.

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1 4. The apparatus as described in claim 1, wherein error coding of a network includes  
 2 a network element.

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1 5. The apparatus as described in claim 4, wherein the network element includes at  
 2 least one of a communication link, switch, router, transmission link and  
 3 interconnect module.

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1 6. The apparatus as described in claim 1, wherein error coding of data storage  
 2 includes a data storage element.

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1 7. The apparatus as described in claim 6, wherein the data storage element includes  
2 at least one of a storage device and a disk array.

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1 8. The apparatus as described in claim 1, wherein the protocol accelerator is suitable  
2 for increasing throughput of at least one of IPv6 and IPv4 Internet protocols.

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1 9. The apparatus as described in claim 1, wherein error control provided by the error  
2 control component is extended over failure points of a network, the failure points  
3 including at least one of communication link, switch, router, transmission link,  
4 interconnect module, storage device and processor.

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1 10. The apparatus as described in claim 9, wherein the network includes at least one  
2 of Internet, Internet 2 and isochronous data transfer network.

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- 1 11. A storage area network (SAN) processor suitable for providing inter-network  
2 storage disposed between a storage device and a network, comprising:  
3 a storage controller;  
4 a network input/output interface suitable for coupling to a network to provide a  
5 network connection;  
6 a storage device input/output interface suitable for coupling to a storage device;  
7 a hybrid switching element suitable for interpreting network data received from a  
8 networking device and storage data received from a storage device;  
9 a protocol accelerator suitable for utilizing a data storage addressing scheme; and  
10 an error control component suitable for compensating for loss of at least one of a  
11 network element and a data storage element;  
12 wherein the error control component is communicatively coupled to the hybrid  
13 switching element, protocol accelerator and storage controller so as to  
14 enable error control coding suitable for describing a data storage element  
15 and a network element accessible to the storage area network (SAN)  
16 processor.
- 1 12. The storage area network (SAN) processor as described in claim 11, wherein data  
2 is addressed utilizing a 128 bit addressing scheme.
- 1 13. The storage area network (SAN) processor as described in claim 12, wherein the  
2 addressing scheme is Ipv6.
- 1 14. The storage area network (SAN) processor as described in claim 11, wherein the  
2 network element includes at least one of a communication link, switch, router,  
3 transmission link and interconnect module.
- 1 15. The storage area network (SAN) processor as described in claim 11, wherein the  
2 data storage element includes at least one of a storage device and a disk array.

1 16. The storage area network (SAN) processor as described in claim 11, wherein the  
2 protocol accelerator is suitable for increasing throughput of at least one of IPv6  
3 and IPv4 Internet protocols.

1 17. The storage area network (SAN) processor as described in claim 11, wherein error  
2 control provided by the error control component is extended over failure points of  
3 a network, the failure points including at least one of communication link, switch,  
4 router, transmission link, interconnect module, storage device and processor.

1 18. The storage area network (SAN) processor as described in claim 17, wherein the  
2 network includes at least one of Internet, Internet 2 and isochronous data transfer  
3 network.

- 1 19. A method of acquiring data, comprising:  
2 receiving a request for storage data, the storage data available on a first storage  
3 device;  
4 determining the storage data on the first storage device is unavailable by a hybrid  
5 switching element, the unavailability of the storage data caused by at least  
6 one of a network failure and a storage device failure;  
7 delineating a path for obtaining the storage data, wherein the path is delineated by  
8 determining a communication pathway and redundant data address; and  
9 acquiring data based on the delineated path.
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1 20. The method as described in claim 19, wherein determining includes utilizing error  
2 control coding.

- 1 21. A storage area network (SAN) processor suitable for providing inter-network  
2 storage disposed between a storage device and a network, comprising:  
3 means for controlling storage;  
4 means for interfacing with a network, the network interfacing means suitable for  
5 coupling to a network to provide a network connection;  
6 means for interfacing with a storage device, the storage device interfacing means  
7 suitable for coupling to a storage device;  
8 means for hybrid switching, the hybrid switching means suitable for interpreting  
9 network data received from a networking device and storage data received  
10 from a storage device;  
11 means for accelerating a protocol, the protocol accelerator means suitable for  
12 utilizing a data storage addressing scheme; and  
13 means for controlling errors, the error control means suitable for compensating for  
14 loss of at least one of a network element and a data storage element;  
15 wherein the error control means is communicatively coupled to the hybrid  
16 switching means, protocol accelerator means and storage controller means  
17 so as to enable error control coding including at least two of  
18 communication links, switches, data storage and processors accessible to  
19 the SAN processor.
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- 1 22. The storage area network (SAN) processor as described in claim 21, wherein data  
2 is addressed utilizing a 128 bit addressing scheme.
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- 1 23. The storage area network (SAN) processor as described in claim 22, wherein the  
2 addressing scheme is at least one of IPv6 and IPv4.
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- 1 24. The storage area network (SAN) processor as described in claim 21, wherein the  
2 network element includes at least one of a communication link, switch, router,  
3 transmission link and interconnect module.
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1 25. The storage area network (SAN) processor as described in claim 21, wherein the  
2 data storage element includes at least one of a storage device and a disk array.

1 26. The storage area network (SAN) processor as described in claim 21, wherein the  
2 protocol accelerator is suitable for increasing throughput of at least one of IPv6  
3 and IPv4 Internet protocols.

1 27. The storage area network (SAN) processor as described in claim 21, wherein error  
2 control provided by the error control component is extended over failure points of  
3 a network, the failure points including at least one of communication link, switch,  
4 router, transmission link, interconnect module, storage device and processor.

1 28. The storage area network (SAN) processor as described in claim 27, wherein the  
2 network includes at least one of Internet, Internet 2 and isochronous data transfer  
3 network.

- 1     29.     An inter-networked storage system, comprising:  
2             a network suitable for transmitting electronic data;  
3             a first node communicatively coupled to the network, the first node including  
4                 a storage device suitable for storing electronic data; and  
5                 a storage/network processor coupled to the storage device, the  
6                     storage/network processor including  
7                     a hybrid switching element suitable for interpreting network data  
8                         received from a networking device and storage data  
9                         received from a storage device;  
10             an addressing component suitable for addressing data in a format  
11                 suitable for storage across the network; and  
12             an error control component suitable for compensating for loss of at  
13                 least one of a network element and a data storage element;  
14             and  
15             a second node communicatively coupled to the first node over the network, the  
16                 second node including  
17                 a storage device suitable for storing electronic data; and  
18                 a storage/network processor coupled to the storage device, the  
19                     storage/network processor including  
20                     a hybrid switching element suitable for interpreting network data  
21                         received from a networking device and storage data  
22                         received from a storage device;  
23                 an addressing component suitable for addressing data in a format  
24                     suitable for storage across the network; and  
25                 an error control component suitable for compensating for loss of at  
26                     least one of a network element and a data storage element  
27     wherein error control coding is provided suitable for describing network error  
28             data and data storage error data to enable the error control components to  
29             provide inter-networked storage over the first node and the second node.



1 30. The inter-networked storage system as described in claim 29, wherein the inter-  
 2 networked storage includes data distributed over a plurality of nodes utilizing a  
 3 128 bit addressing scheme.

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1 31. The inter-networked storage system as described in claim 30, wherein the  
 2 addressing scheme is at least one of IPv6 and IPv4.

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1 32. The inter-networked storage system as described in claim 29, wherein error  
 2 coding of a network includes a network element.

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1 33. The inter-networked storage system as described in claim 32, wherein the network  
 2 element includes at least one of a communication link, switch, router,  
 3 transmission link and interconnect module.

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1 34. The inter-networked storage system as described in claim 29, wherein error  
 2 coding of data storage includes a data storage element.

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1 35. The inter-networked storage system as described in claim 34, wherein the data  
 2 storage element includes at least one of a storage device and a disk array.

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1 36. The inter-networked storage system as described in claim 29, wherein the  
 2 protocol accelerator is suitable for increasing throughput of Ipv6 Internet  
 3 protocol.

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1 37. The inter-networked storage system as described in claim 29, wherein error  
 2 control provided by the error control component is extended over failure points of  
 3 a network, the failure points including at least one of communication link, switch,  
 4 router, transmission link, interconnect module, storage device and processor.

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- 1 38. The inter-networked storage system as described in claim 37, wherein the network  
2 includes at least one of Internet, Internet 2 and isochronous data transfer network.

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